Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A camera for high-speed image processing, comprising:

a photodetector array having a plurality of photodetectors, which are arranged two-dimensionally in a plurality of rows and in a plurality of columns and which are divided into a plurality of blocks, the photodetector array repeatedly receiving optical images and generating output signals for the optical images in a plurality of consecutive frames at a predetermined frame rate;

an analog-to-digital converter array receiving, from the photodetector array, the output signals for the optical images in the plurality of consecutive frames and generating digital signals in the plurality of consecutive frames, the analog-to-digital converter array including a plurality of analog-to-digital converters in one-on-one correspondence with the plurality of blocks in the photodetector array, each analog-to-digital converter performing analog-to-digital conversion of the output signals which are read sequentially from the photodetectors in the corresponding block;

an image-processing unit performing predetermined processes on the plurality of consecutive frames of the digital signals, which are successively transferred from the analog-to-digital converter array and which correspond to the signals outputted from the photodetectors, thereby generating processed result signals, other than the output signals for the optical signals, indicating the results of the processes on the plurality of consecutive frames;

a selector selecting, among the plurality of consecutive frames, at least one frame based on the processed result signals for the plurality of consecutive frames obtained by the image-processing unit;

a signal converter converting, into an image signal of a desired frame rate, at least one of the processed result signal and the ~~output~~ digital signal from the analog-to-digital converter array, the signal converter outputting the image signal; and

a signal conversion controller controlling the signal converter to perform the image signal conversion operation for the at least one frame selected by the selector.

2. (Original) A camera for high-speed image processing as claimed in claim 1, wherein the desired frame rate is lower than the predetermined frame rate.

3. (Previously Presented) A camera for high-speed image processing as claimed in claim 1, wherein the signal converter converts either one of the digital signal from the analog-to-digital converter array and the processed result signal, into the image signal of the desired frame rate, and outputs the image signal.

4. (Previously Presented) A camera for high-speed image processing as claimed in claim 1, wherein the signal converter combines the digital signal from the analog-to-digital converter array and the processed result signal, converts the combined signal into the image signal of the desired frame rate, and outputs the image signal.

5. (Previously Presented) A camera for high-speed image processing as claimed in claim 1, wherein the signal converter has a buffer memory at a signal input side thereof, the buffer memory storing at least one of the digital signal from the analog-to-digital converter array for at least several frames and the processed result signal for the at least several frames.

6. (Original) A camera for high-speed image processing as claimed in claim 1, further comprising a data buffer storing predetermined process data, the image-processing unit performing a predetermined parallel process, using the predetermined process data, onto the digital signals that are transferred from the analog-to-digital converter array and that correspond to the signals outputted from the photodetectors.

7. (Original) A camera for high-speed image processing as claimed in claim 1, wherein the plurality of analog-to-digital converters in the analog-to-digital converter array are provided in one-on-one correspondence with the plurality of rows of photodetectors in the photodetector array.

8. (Original) A camera for high-speed image processing as claimed in claim 1, wherein the plurality of analog-to-digital converters in the analog-to-digital converter array are provided in one-on-one correspondence with the plurality of columns of photodetectors in the photodetector array.

9. (Original) A camera for high-speed image processing as claimed in claim 1, wherein the image-processing unit includes a plurality of processors in one-to-one correspondence with the plurality of photodetectors, the plurality of processors performing parallel processes on the digital signals that are transferred from the analog-to-digital converter array and that correspond to the signals outputted from the plurality of photodetectors.

10. (Currently Amended) A camera for high-speed image processing as claimed in claim 1, wherein the image-processing unit includes at least one parallel processing circuit, each of the at least one parallel processing circuit performing a corresponding parallel process on the digital signals that are transferred from the analog-to-digital converter array and that correspond to the signals outputted from the photodetectors, thereby outputting a processed result signal indicative of the processed result, the selector selecting at least one frame based on at least one process result from the at least one parallel processing circuit, the signal converter converting at least one of the ~~output~~ digital signal from the analog-to-digital converter array and the processed result signal obtained by the at least one parallel processing circuit, into the image signal of the desired frame rate, and outputting the image signal.

11. (Original) A camera for high-speed image processing as claimed in claim 10, wherein each of the at least one parallel processing circuit is provided with several processing elements in one-to-one correspondence with several blocks that make up at least a portion of all the plurality of blocks in the photodetector array, each of the several processing elements performing a predetermined parallel process on the digital signals that are transferred from the corresponding analog-to-digital converter and that are equivalent to the signals outputted from the photodetectors existing in the corresponding block.

12. (Original) A camera for high-speed image processing as claimed in claim 10, wherein the plurality of analog-to-digital converters in the analog-to-digital converter array are provided in one-to-one correspondence with the plurality of rows of photodetectors in the photodetector array, each of the at least one parallel processing circuits including several processing elements which are provided in one-to-one correspondence with several rows that make up at least a portion of all the plurality of rows in the photodetector array, each of the several processing elements performing a predetermined parallel process on digital signals that are transferred from the analog-to-digital converter array and that are equivalent to the signals outputted from the photodetectors in the corresponding row.

13. (Previously Presented) A camera for high-speed image processing as claimed in claim 1, wherein the selector selects at least one frame that includes one frame, processed results thereof obtained by the image-processing unit satisfying a predetermined condition.

14. (Previously Presented) A camera for high-speed image processing as claimed in claim 13, wherein the selector judges whether or not the processes results for the consecutive frames satisfy the predetermined condition, determines one frame, processed results thereof satisfying the predetermined condition, and selects at least one frame including the determined one frame.

15. (Previously Presented) A camera for high-speed image processing as claimed in claim 1, wherein the image processing unit performs a characteristic extracting process on the plurality of consecutive frames of the digital signals to determine characteristics of the consecutive frames, and

wherein the selector judges whether or not the extracted characteristics of the consecutive frames satisfy the predetermined condition, determines one frame, a characteristic thereof satisfying the predetermined condition, and selects at least one frame including the determined one frame.

16. (Previously Presented) A camera for high-speed image processing as claimed in claim 15, wherein the image processing unit performs a center of gravity calculation process on the plurality of consecutive frames of the digital signals to determine the locations of the centers of gravity in the consecutive frames of the digital signals, and

wherein the selector judges whether or not the locations of centers of gravity in the consecutive frames satisfy the predetermined condition, determines one frame, locations of the center of gravity thereof satisfying the predetermined condition, and selects at least one frame including the determined one frame.

17. (Previously Presented) A camera for high-speed image processing as claimed in claim 15, wherein the image processing unit performs a pattern matching process on the plurality of consecutive frames of the digital signals to generate the processed result signals indicating whether or not a predetermined pattern is detected in the consecutive frames, and

wherein the selector determines, based on the process result signals, one frame in which the predetermined pattern is detected, and selects at least one frame including the determined one frame.

18. (Previously Presented) A camera for high-speed image processing as claimed in claim 1, wherein the image-processing unit includes a parallel processing circuit that

performs a parallel process on the plurality of consecutive frames of the digital signals to generate the processed result signals indicative of whether or not the consecutive frames of the digital signals satisfy a predetermined condition, and

wherein the selector selects at least one frame that includes one frame, a processed result signal thereof indicating that the subject frame satisfies the predetermined condition.

19. (Previously Presented) A camera for high-speed image processing as claimed in claim 18, wherein the parallel processing circuit performs a center of gravity calculation process on the plurality of consecutive frames of the digital signals to generate the processed result signals indicative of the locations of the centers of gravity in the consecutive frames of the digital signals, and

wherein the selector judges, based on the processed result signals, whether or not the locations of centers of gravity of the consecutive frames satisfy the predetermined condition, determines one frame, locations of the center of gravity thereof satisfying the predetermined condition, and selects at least one frame including the determined one frame.

20. (Previously Presented) A camera for high-speed image processing as claimed in claim 18, wherein the parallel processing circuit performs a pattern matching process on the plurality of consecutive frames of the digital signals to generate the processed result signals indicating whether or not a predetermined pattern is detected in the consecutive frames, and

wherein the selector determines, based on the processed result signals, one frame in which the predetermined pattern is detected, and selects at least one frame including the determined one frame.